REMARKS

Claims 1-14 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Belkin et al. (U.S. Patent Number 6,567,912, hereinafter "Belkin"). Respectfully disagreeing with these rejections, reconsideration is requested by the applicants.

Independent claim 1 recites "when the first peripheral component, while initializing, **locks up a bus that the controller component and the plurality of peripheral components share.**" Independent claim 8 recites "a bus to which the first peripheral and the second peripheral are connected; and... when the first peripheral, while initializing, **locks up the bus.**" The Examiner appears to assert that the watch-dog timer expiring in Belkin teaches this claim language. However, Belkin discusses the buses in his system at column 1, lines 50 – 65, which reads as follows (emphasis added):

> In FIG. 1, a block diagram of a computer system 100 having a controller and multiple devices in accordance with an embodiment of the invention is shown. The system 100 has an input device 102 coupled by a data **bus** and address **bus** to a controller 104 and a Random Access Memory 108 (RAM). The controller 104 is coupled to the input device 102, read only memory (ROM) 106, RAM 108, an activity or watch dog timer 110, device one 112, device two 114, and device three 116. In the current embodiment the devices are shown as residing within the system, but in alternate embodiments the devices may selectively be independent single board computers coupled to the controller by an external **bus**. The above elements are all coupled together by an address **bus** and a data **bus**. Additionally, stored in the RAM 106 is an area 118 for a plurality of boot routines 124, 128, 130, 132, boot marker 120, and a boot list table 122.

Although Belkin discusses buses in his system, the applicants do not understand Belkin to teach a bus locking up when a peripheral is initializing, as claimed.

Independent claim 1 recites "determining that an **identifier** of the first peripheral component was **not stored.**" Independent claim 8 recites "determining that an **identifier** of the first peripheral was **not stored.**" The Examiner appears to assert that storing either a pass or fail status in Belkin teaches this claim language. However, the applicants submit that storing a "fail" to indicate a failed boot attempt does not teach or

suggest determining that an **identifier** of a peripheral component was **not stored**. In the present application, the identifier of an initializing peripheral component is not stored because the bus that the controller component and the peripheral component share is locked up. Thus, a determination is being made of whether the bus locked up last time the peripheral component initialized, not just whether a failed status was stored.

Independent claim 1 recites "**skipping** the first peripheral component in the power-up sequence as a result of the step of determining **to prevent the bus from being locked up.**" Independent claim 8 recites "a controller...arranged to restart the power-up sequence and **skip** the first peripheral in the power-up sequence as a result of determining that an identifier of the first peripheral was not stored when the first peripheral, while initializing, **locks up the bus**." The Examiner appears to assert that not attempting to initialize a device more than two times, as in Belkin, teaches this claim language.

However, the applicants submit that Belkin not only does not teach or suggest skipping the first peripheral component in the power-up sequence but Belkin teaches the opposite. As the Examiner points out, Belkin teaches attempting to initialize those devices, and only those devices, that failed their first initialization attempt. The present application claims the opposite. When the first peripheral component, while initializing, locks up a bus that the controller component and the plurality of peripheral components share, the power-up sequence is restarted, and the first peripheral component in the power-up sequence is **skipped** (as a result of the step of determining that an identifier of the first peripheral component was not stored) in order **to prevent the bus from being locked up again**. If the teaching of Belkin, as cited by the Examiner, were applied to an embodiment of the present application, the peripheral component that locked up the bus the first time would be powered up for another chance to lock up the bus and force yet another power-up sequence restart. This is contrary to the problem the present application addresses. The applicants refer the Examiner to the abstract of the present application, for example:

> To address the need for a high availability system (100) and method of initializing that address failures that lock up common communication buses (109) in these systems, the present invention avoids powering-up peripheral components (e.g., 102-103) that have

previously locked up the bus. It accomplishes this by storing indicators of successful initializations in memory (105), and then subsequently powering-up components only if such an indicator was stored for that component's last power-up.

Since none of the references cited, either independently or in combination, teach all of the limitations of independent claims 1 or 8, or therefore, all the limitations of their respective dependent claims, it is asserted that neither anticipation nor a prima facie case for obviousness has been shown. No remaining grounds for rejection or objection being given, the claims in their present form are asserted to be patentable over the prior art of record and in condition for allowance. Therefore, allowance and issuance of this case is earnestly solicited.

The Examiner is invited to contact the undersigned, if such communication would advance the prosecution of the present application. Lastly, please charge any additional fees (including extension of time fees) or credit overpayment to Deposit Account No. **502117 -- Motorola, Inc.**

Respectfully submitted,
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